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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/001,683	10/25/2001	Jeffrey M. Calvert	50765	3177

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EXAMINER	
MUTSCHLER, BRIAN L	

ART UNIT	PAPER NUMBER
1753	

DATE MAILED: 03/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/001,683	CALVERT ET AL.	
	Examiner	Art Unit	
	Brian L. Mutschler	1753	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-19 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-19 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 25 October 2001 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 20011025.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Comments

1. The Examiner notes that the methods recited in the claims are disclosed by the Applicant as known methods, such as disclosed by EP 1 005 078 A1 and WO 99/47731 (see pages 1-3, 10, 12, and 13 of the instant disclosure). The instant claims recite the use of these methods in the alternative depending upon a testing step to determine if voids are present in the attempted method; when a void is detected, one of the other methods is attempted. Since the method requires a minimum of a single electroplating method and a single testing step, it appears that the novelty of the invention is the step of testing the electroplated device for voids.

Drawings

2. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

3. Claims 1 and 12 are objected to because of the following informalities:

   a. In claim 1 at line 2, please change "seed layer comprising, comprising" to --seed layer, comprising--.

   b. In claim 12 at line 1, please change "the method" to --The method--.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 2 and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Sakamoto et al. (U.S. Pat. No. 5,788,830).

Regarding claims 1 and 14, Sakamoto et al. disclose a method for electroplating a plurality of electronic devices, which have through-holes (apertures) (col. 1, lines 6-10). Each device has a surface comprising copper or a copper alloy, which is equivalent to the seed layer recited in the instant claims (col. 2, lines 2-24; col. 3, line 56 to col. 4, line 3). A metal layer is electroplated on the copper or copper alloy layer to create a void-free layer, which includes the interior of the through-holes (col. 5, lines 30-54). The device is then tested using a backlight test and a solder shock test, substituting oil for solder, to ascertain that the plating layer is void free (col. 7, lines 44-51). Since the electroplating process disclosed creates void-free electroplating layers, the process is sufficient to electroplate devices without voids, i.e., there is no need to continue with alternative methods.

Regarding claim 2, the conductive layer (seed layer) is comprised of copper or copper alloy (col. 2, lines 2-24).

Since Sakamoto et al. teaches the minimum process limitations required in the limitations of the instant claims, the reference is deemed to be anticipatory.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-5, 7-11, 13-16, 18, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over EP 1 005 078 A1, herein referred to as EP '078, in view of either Sakamoto et al. (U.S. Pat. No. 5,788,830) or Carano et al. (U.S. Pat. No. 6,375,731).

Regarding claims 1, 8, 14, and 19, EP '078 discloses a method of electroplating electronic devices, wherein each device has openings with high aspect ratios and a copper-containing seed layer (col. 3, lines 21-31). A cathodic activation step reduces copper oxide on the seed layer (col. 4, lines 37-58). A copper film is electroplated over the seed layer (col. 6, lines 18-35). The cathodic activation step reduces the likelihood of void formation and allows the plating of material within the opening "without having to worry about void formation" (col. 7, lines 19-23).

Regarding claim 2, the seed layer comprises copper and copper oxide (col. 5, line 58 to col. 6, line 5).

Regarding claims 3, 9, and 15, the electronic devices comprise wafers (col. 3, lines 34-38).

Regarding claims 4, 10 and 16, the device further comprises a barrier layer (col. 3, lines 48-52).

Regarding claims 5 and 11, the barrier layer may comprise tantalum, titanium, molybdenum, cobalt, nitrides of those materials, or the like (col. 3, lines 48-52).

Regarding claims 7, 13, and 18, the openings have an aspect ratio of at least 2:1 (col. 3, lines 45-47).

The method of EP '078 differs from the instant invention because EP '078 does not disclose a step of testing the electronic device for voids, and if voids are found, using additional seed repair steps, as recited in claims 1, 8, 14, and 19.

EP '078 discloses that the electroplated have a low likelihood of voids (col. 7, lines 19-23). In order to determine if the electroplated layers have a low likelihood of voids, some form of test must be performed to determine the presence or absence of voids. Both Sakamoto et al. and Carano et al. disclose the use of tests to test for voids. Sakamoto et al. teach the use of backlight tests and solder shock tests to test for voids (col. 7, lines 44-51). Carano et al. teach the use of a hot oil thermal shock test to test for voids (col. 7, lines 58-62).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have modified the method of EP '078 to test the electroplated layer for voids to confirm that the electroplated layers are indeed void-free as taught by Sakamoto et al. and Carano et al. because voids can decrease the reliability of electronic devices and testing for voids determines that the voids are not present.

Since the method of EP '078 does not create voids, seed layer repair steps are not necessary, and the combination meets the minimum process limitations required by the instant claims.

8. Claims 6, 12, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over EP 1 005 078 A1 in view of either Sakamoto et al. (U.S. Pat. No. 5,788,830) or Carano et al. (U.S. Pat. No. 6,375,731), as applied above to claims 1-5, 7-11, 13-16, 18, and 19, and further in view of either Reid (U.S. Pat. No. 6,024,857) or Andricacos et al. (U.S. Pat. No. 6,395,164).

EP '078 and Sakamoto et al. or Carano et al. describe a method having the limitations recited in claims 1-5, 7-11, 13-16, 18, and 19, as explained above in section 7. EP '078 further teaches, "Semiconductor devices continue to be shrunk to smaller dimensions" (col. 1, lines 12-14).

The method described by EP '078 and Sakamoto et al. or Carano et al. differs from the instant invention because they do not disclose that the apertures have a width less than or equal to 1 μm, as recited in claims 6, 12, and 17.

Reid discloses an electroplating method for plating void-free metal layers within apertures having aspect ratios of 4:1 or greater and dimensions less than 0.25 μm (col. 3, lines 4-12; col. 8, lines 12-30).

Andricacos et al. disclose a seed repair method for forming a seed layer that is subsequently electroplated (col. 1, lines 42-51). The method is used for apertures

having dimensions less than 0.25 μm and aspect ratios greater than 3:1 (col. 1, lines 28-33).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have used the method described by EP '078 and Sakamoto et al. or Carano et al. to plate apertures having a width of less than 1 μm as taught by both Reid and Andricacos et al. because smaller apertures lead to faster and smaller electronic devices and Reid and Andricacos et al. teach that such apertures can be similarly electroplated in a void-free manner.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. U.S. Pat. No. 6,197,181 issued to Chen.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian L. Mutschler whose telephone number is (571) 272-1341. The examiner can normally be reached on Monday-Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nam Nguyen can be reached on (571) 272-1342. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

blm
February 3, 2004

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SUPERVISORY PATENT EXAMINER
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